25/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07163881 **Image available**
CACHE ACCESS CONTROL SYSTEM AND DATA PROCESSING SYSTEM

PUB. NO.: 2002-032265 [JP 2002032265 A]
PUBLISHED: January 31, 2002 (20020131)
INVENTOR(s): HOSOYA MUTSUMI
YAMAMOTO MICHITAKA
APPLICANT(s): HITACHI LTD
APPL. NO.: 2000-213803 [JP 2000213803]
FILED: July 14, 2000 (20000714)
INTL CLASS: G06F-012/08

ABSTRACT

PROBLEM TO BE SOLVED: To provide a method for dynamically specifying an exclusive/shared area and to always perform optimal **cache** coincidence control.

SOLUTION: An **L1** **cache** consisting of **L1** data (a data array) and dir (a directory) are provided in processors IP0 to IPn, plural **L2** **caches** are connected with the respective **L1** **caches** and the **L2** **caches** are connected with a main memory **L3** . An SCHC (**L2** **cache** reference **history** control part) inputs pieces of **L2** **cache** state information 360 and **L2** **cache** access request 370 from the **L2** **caches** and discriminate their attributes (exclusive areas or shared areas) by every line of **L2** . An SCCC (**coincident** control part) performs the **coincident** control of the respective **L2** **caches** by an invalid type protocol or an update type protocol based on the attributes. The attributes are discriminated as the shared areas only when a line shared by the plural **L2** **caches** in the **past** is accessed again after being once cancelled by the invalid type protocol.

25/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

07022174 **Image available**
PREDICTION INFORMATION MANAGING METHOD

PUB. NO.: 2001-249806 [JP 2001249806 A]
PUBLISHED: September 14, 2001 (20010914)
INVENTOR(s): JAMES E MCCORMIC JR
STEPHEN R ANDY
APPLICANT(s): HEWLETT PACKARD CO (HP)
APPL. NO.: 2001-043880 [JP 2001043880]
FILED: February 20, 2001 (20010220)
PRIORITY: 00 510049 [US 2000510049], US (United States of America), February 22, 2000 (20000222)
INTL CLASS: G06F-009/38; G06F-012/08

ABSTRACT

PROBLEM TO BE SOLVED: To provide an efficient means to manage instructions and branching **prediction** information about the instructions of a computer processor.

SOLUTION: When **prediction** information is stored in memory hierarchy at **plural** **levels** including low **level** and high **level** **prediction** **caches** and a **predicted** information value is fetched from the low level **prediction** cache and when no **predicted** information value is stored there, the **predicted** information value is fetched from the high level **prediction** cache. Pieces of the **prediction** information stored in the low level and high level **prediction** caches are periodically updated by

using the **prediction** information stored in the low level **prediction** cache. Furthermore, efficiency of management of the instruction and the branching **prediction** information is enhanced by integrating the low level **prediction** cache with a low level instruction cache and controlling them under common management mechanism.

25/5/3 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

[illegible] **Image available**
METHOD FOR MAINTAINING CACHE COHERENCE, AND COMPUTER SYSTEM

PUB. NO.: 11-328027 [JP 11328027 A]
PUBLISHED: November 30, 1999 (19991130)
INVENTOR(s): ARIMILLI RAVI KUMAR
DODSON JOHN STEVEN
LEWIS JERRY DON
APPLICANT(s): INTERNATL BUSINESS MACH CORP <IBM>
APPL. NO.: 11-031787 [JP 9931787]
FILED: February 09, 1999 (19990209)
PRIORITY: 24394 [US 24394], US (United States of America), February 17, 1998 (19980217)
24614 [US 24614], US (United States of America), February 17, 1998 (19980217)
INTL CLASS: G06F-012/08; G06F-012/08

ABSTRACT

PROBLEM TO BE SOLVED: To obtain a cache coherence protocol which uses a tagged coherence state to increase the memory band width without immediately writing back a change value to a system memory.
SOLUTION: When a tagged state is assigned to a cache line which is loaded with the change value latest, the **history** state related to the tagged state which is moved between caches (in the horizontal direction) can be used furthermore. This system is also applied to a multi-processor computer system having clustered processing units, and a tagged state is applied t[illegible] of cache lines in each group of **caches** which support **different** processing unit clusters. Priority **levels** are assigned to **different** **cache** states, and they include tagged states for response to requests [illegible] access corresponding memory blocks. Because of use of a crossbar, a tagged intermediary response is transferred to only selected caches which are affected by this intermediary response.

25/5/4 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

04167093 **Image available**
PARALLEL **CACHE** MEMORY

PUB. NO.: 05-158793 [JP 5158793 A]
PUBLISHED: June 25, 1993 (19930625)
INVENTOR(s): SAKAI HIROSHI
APPLICANT(s): AGENCY OF IND SCIENCE & TECHNOL [000114] (A Japanese Government or Municipal Agency), JP (Japan)
APPL. NO.: 03-348383 [JP 91348383]
FILED: December 05, 1991 (19911205)
INTL CLASS: [5] G06F-012/08; G06F-012/08
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 1627, Vol. 17, No. 560, Pg. 24, October 08, 1993 (19931008)

ABSTRACT

PURPOSE: To save the load of a memory bus by providing a function which **predicts** a write request at each **cache** memory.

CONSTITUTION: This device is equipped with **cache** memories 10-12 connected to plural processors **1 - 3** , and connected respectively through a memory bus 13 to a shared memory 14. Each **cache** memory 10-12 **predicts** a write after a read by the processor by comparing a value stored in a register 109 with the value of a register 110. The **cache** memory which receives the transferring request of **cache** line data from the **cache** memory of the processor which issues the read request, invalidates the **cache** line data at the time of **predicting** the write request for its own **cache** line. And also, the **cache** memory of the processor which issues the read request, stores the absence of the **cache** line data in the other **cache** memory at the time of **predicting** the write request of the **cache** line data transferred from the other **cache** memory or the shared memory.

25/5/5 (Item 1 from file: 350)

015249537 **Image available**
WPI Acc No: 2003-310463/200330
XRPX Acc No: N03-247015

Data cache miss lookaside buffer circuit for data processing system, provides predicted **values stored in buffer to execution circuit, when retrieval of value requested by load instruction misses cache**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: LIPASTI M H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6487639	B1	20021126	US 99232262	A	19990119	200330	B

Priority Applications (No Type Date): US 99232262 A 19990119
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6487639	B1		11	G06F-012/00	

Abstract (Basic): US 6487639 B1

NOVELTY - A buffer (60) stores a **predicted** value for the load instruction. A control circuit (62) provides the stored **predicted** value to an execution circuit for processing load instruction, when retrieval of the value requested by the instruction misses the cache (50) in a memory. The value requested by the load instruction is the data to be returned as the result of the instruction.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

(1) Integrated circuit device comprising data cache miss lookaside buffer circuit;

(2) data processing system comprising data cache miss lookaside buffer circuit;

(3) hardware definition program for defining data cache miss lookaside buffer circuit; and

(4) hardware definition program executing method.

USE - For retrieving data from data **cache** in **multilevel** memory architecture used in data processing system such as multiuser computer system e.g. network server, midrange computer e.g. AS/400 computer from international business machines corporation, main frame computer, single user computer system e.g. workstation computer, desktop computer, portable computer, computing device e.g. embedded controller, etc.

ADVANTAGE - The **predicted** values associated with load instruction which miss the data cache, are limited and the most used and greatest potential latency instruction are **predictable** , thereby reducing the cost of buffer and increasing utilization efficiency of value **prediction** for given size buffer.

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of the data cache miss lookaside buffer circuit.
cache (50)
buffer (60)
control circuit (62)
pp; 11 DwgNo 3/6
Title Terms: DATA; CACHE; MISS; BUFFER; CIRCUIT; DATA; PROCESS; SYSTEM; **PREDICT** ; VALUE; STORAGE; BUFFER; EXECUTE; CIRCUIT; RETRIEVAL; VALUE; REQUEST; LOAD; INSTRUCTION; MISS; CACHE
Derwent Class: T01; U14
International Patent Class (Main): G06F-012/00
File Segment: EPI

25/5/6 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014405656 **Image available**
WPI Acc No: 2002-226359/200228
XRPX Acc No: N02-173708
Method and equipment for controlling uniformity of treatment of substrate surface by action of particle beam, which includes measuring emitted photons, for use in microelectronics
Patent Assignee: X-ION (XION-N); X-ION SA (XION-N)
Inventor: BORSONI G; LE ROUX V; VALLIER L
Number of Countries: 094 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200165596	A2	20010907	WO 2001FR486	A	20010220	200228	B
AU 200135718	A	20010912	AU 200135718	A	20010220	200228	
FR 2805925	A1	20010907	FR 20002617	A	20000301	200230	

Priority Applications (No Type Date): FR 20002617 A 20000301
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200165596	A2	F	14	H01L-021/66	
AU 200135718	A			H01L-021/66	Based on patent WO 200165596
FR 2805925	A1			H01L-021/66	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

Abstract (Basic): WO 200165596 A2
NOVELTY - The method for the control of uniformity of treatment of the surface layer (101) of a semiconductor wafer (100) with substrate (102) by particle beam (F) of e.g. Argon ions includes an instantaneous measurement of the number of photons (1) emitted due to the interaction of particles with the surface and is carried out in connection with the detection by imaging in each elementary zone of the surface as defined on the basis of the resolution of formed image and in the course of all treatment. A variation in measurement is determined as a function of the position of emission zones in order to determine an average of the spatial distribution of the emission intensity and to measure a fault in the uniformity of treatment proportionally to the difference with respect to the average.
DETAILED DESCRIPTION - A step of adjustment or stop of treatment to set off when the fault in uniformity is greater than a predetermined critical value. A step of measuring the energy of photons detected locally is provided in order to follow the advance of treatment and to adjust or stop the treatment when the energy variation exceeds a predetermined difference in a given period. A step of measuring the total number of photons for at least **one** energy **level** is provided. An analysis of spatial distribution of emission intensity determines the local fault of uniformity and a modulation of beam scanning

required to correct the fault. The means for selecting particles in velocity and direction are subjected to the analysis of spatial distribution, and comprise collimation which selects particles in direction. The measurement of uniformity of treatment is recorded for **historic** tracing of parameters in successive applications to each wafer passing in the production line. The equipment comprises a photon detector (103) which forms a digital image and is connected to a signal processing and data management unit (104). The photon detector is a digital camera or photo-digital apparatus equipped with a charge-coupled device (CCD) for intensity measurements, where the wavelength of light emitted from each elementary zone of treated surface corresponds to each pixel, and after calibration, to the number of photons received by each pixel. An evolution of intensity of dominant colors is determined in order to follow the evolution of treatment. The photon detector is cooled by a device operated by the Peltier effect, or by a cryogenic fluid. The means for selecting particles are controlled by the unit (104) as a function of measurements and comprises a set of adjustable **caches** for local adjustments of particle flux in order to compensate the uniformity fault. The photon detector is zoom-focused on a part of treated surface in order to increase the resolution, and the scanning by photon detector is **synchronized** with the scanning by ion beam. The photon detector is mounted on a motorized platform and is subjected to successively irradiated zones. Several monochromatic photon detectors are utilized in combination with a wavelength separator.

USE - In methods for treatment of surface of a substrate such as semiconductor wafer by projecting multi charge ion beam, used in a number of applications, such as the formation of layer of gate oxide, cleaning and preparation of surface, the exposure through mask and the etching of dielectric layer in producing micro-patterns of integrated circuits, and the formation of nano-points of silicon oxide by flash exposure in order to form the quantum-effect components; by use of ions from e.g. an electron cyclotron resonance (ECR) source.

ADVANTAGE - The surface treatment is controlled in real time, and the uniformity is improved to a precision of the order of micrometer.

DESCRIPTION OF DRAWING(S) - The drawing is a schematic view of the equipment.

Emitted photons (1)
Wafer (100)
Surface layer (101)
Substrate (102)
Photon detector (103)
Signal processing and data management unit (104)
pp; 14 DwgNo 1/2

Title Terms: METHOD; EQUIPMENT; CONTROL; UNIFORM; TREAT; SUBSTRATE; SURFACE ; ACTION; PARTICLE; BEAM; MEASURE; EMIT; PHOTON; MICROELECTRONIC
Derwent Class: S03; U11; V05
International Patent Class (Main): H01L-021/66
International Patent Class (Additional): C23C-014/48; C23C-014/54; G01B-015/08; H01L-021/265
File Segment: EPI

25/5/7 **(Item 3 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

014095080
WPI Acc No: 2001-579294/200165
Related WPI Acc No: 1999-404078; 1999-518192
XRPX Acc No: N01-431144

Power consumption reduction method for microprocessor with multiple levels **of** cache **involves miss** prediction **of lower level cache based on fact that misses occur in bursts corresponding to changes in working data set**

Patent Assignee: NAT SEMICONDUCTOR CORP (NASC)
Inventor: MUSOLL E
Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6282614	B1	20010828	US 99292541	A	19990415	200165	B

Priority Applications (No Type Date): US 99292541 A 19990415
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6282614	B1		11	G06F-009/44	

Abstract (Basic): US 6282614 B1

NOVELTY - Higher level cache inhibited if hit **predicted** in current level. Window of given size defined e.g. S. If miss occurs, device (8) **predicts** next miss will occur in next S accesses. If no miss occurs in these accesses, hit **predicted** until next miss occurs.

DETAILED DESCRIPTION - Power reduction is achieved by inhibiting pre-charging of bit lines of higher level cache and by keeping address input to that cache at same value as previous access. An INDEPENDENT CLAIM is included for circuits to implement the described power consumption reduction method.

USE - Power consumption reduction method for microprocessor with **multiple levels** of **cache** (claimed).

ADVANTAGE - Reduces power consumption in a multiple cache microprocessor without creating an unacceptable reduction in processing speed.

DESCRIPTION OF DRAWING(S) - **Prediction** device (8)
Hit/miss detection circuit (10)
Counter (12)
Comparison circuit (14)
Prediction circuit (16)
pp; 11 DwgNo 0/10

Title Terms: POWER; CONSUME; REDUCE; METHOD; MICROPROCESSOR; MULTIPLE; LEVEL; CACHE; MISS; **PREDICT** ; LOWER; LEVEL; CACHE; BASED; FACT; MISS; OCCUR; BURST; CORRESPOND; CHANGE; WORK; DATA; SET
Derwent Class: T01
International Patent Class (Main): G06F-009/44
International Patent Class (Additional): G06F-012/00
File Segment: EPI

25/5/8 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012598661 **Image available**
WPI Acc No: 1999-404767/199934
XRPX Acc No: N99-301724

Cache memory controlling method using independently executable sequences of instructions (Threads)

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: AVERILL D A; BORKENHAGEN J M
Number of Countries: 029 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9927452	A1	19990603	WO 98US25001	A	19981119	199934	B
US 6263404	B1	20010717	US 97976533	A	19971121	200142	
TW 460798	A	20011021	TW 98119101	A	19981118	200248	

Priority Applications (No Type Date): US 97976533 A 19971121
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9927452	A1	E	70	G06F-012/08	
				Designated States (National): CA CN CZ HU IL JP KR PL RU	
				Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE	
US 6263404	B1			G06F-012/08	
TW 460798	A			G06F-015/00	

Abstract (Basic): WO 9927452 A1

NOVELTY - Cache memory sequencers (50) speculatively **predict** location of memory, forwarding contents requested by processor from cache while verifying correctness. When not duplicated in cache (miss), sequencer manages return of memory contents, after being accessed from main memory (12), to cache buffer, by hardware multithreading, and the sequencer is disabled when cache linefill completed.

DETAILED DESCRIPTION - Processor rapidly accesses memory location when main memory duplicated in cache (cache hit). When not duplicated in cache, three sequencers manage return of memory contents to **cache** buffer by hardware multithreading, after being accessed. **Different cache levels** are used. **Two** threads are used. An independent claim includes storage control unit.

USE - Routing memory contents for execution by processor.

ADVANTAGE - Reduces latency. Reduces memory access delays.

DESCRIPTION OF DRAWING(S) - The drawing shows block diagram of part of storage control unit.

main memory (12)

sequencers (50)

pp; 70 DwgNo 1B/4

Title Terms: CACHE; MEMORY; CONTROL; METHOD; INDEPENDENT; EXECUTE; SEQUENCE ; INSTRUCTION; THREAD

Derwent Class: T01

International Patent Class (Main): G06F-012/08; G06F-015/00

File Segment: EPI

25/5/9 **(Item 5 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

011495474 **Image available**

WPI Acc No: 1997-473387/199744

XRPX Acc No: N97-394683

Branch prediction method in multi - level cache system - in which branch prediction information associated with overwritten cache entry is stored in next level cache when cache line is victimised

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)

Inventor: YUNG R

Number of Countries: 005 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 798632	A2	19971001	EP 97301124	A	19970221	199744	B
EP 798632	A3	19971008	EP 97301124	A	19970221	199813	
JP 10055276	A	19980224	JP 9788685	A	19970325	199818	
KR 97066889	A	19971013	KR 9710034	A	19970324	199842	
EP 798632	B1	20020911	EP 97301124	A	19970221	200264	
DE 69715280	E	20021017	DE 615280	A	19970221	200276	
			EP 97301124	A	19970221		

Priority Applications (No Type Date): US 96621418 A 19960325

Cited Patents: No-SR.Pub; 1.Jnl.Ref; EP 318778; US 4679141; US 5163140; US 5423011

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 798632	A2	E	8	G06F-009/38	
Designated States (Regional): DE FR GB					
EP 798632	A3			G06F-009/38	
JP 10055276	A		7	G06F-009/38	
KR 97066889	A			G06F-012/08	
EP 798632	B1	E		G06F-009/38	
Designated States (Regional): DE FR GB					
DE 69715280	E			G06F-009/38	Based on patent EP 798632

Abstract (Basic): EP 798632 A

The method of operating a computer system having multiple cache memories involves storing branch **prediction** information in a first cache memory, writing over an old cache entry with a new cache entry and saving branch **prediction** information from the first cache

corresponding to the old cache entry to a second cache memory.

The method provides a mechanism for restoring the branch **prediction** information upon a cache fill or context switch, thereby eliminating any additional latency for branch **prediction** in connection with a context switch.

USE - Providing reduced latency in multi-threading applications, including lightweight processing which allows context switching without saving full context.

Dwg.1/6

Title Terms: BRANCH; **PREDICT** ; METHOD; MULTI; LEVEL; CACHE; SYSTEM; BRANCH ; **PREDICT** ; INFORMATION; ASSOCIATE; CACHE; ENTER; STORAGE; LEVEL; CACHE; CACHE; LINE

Derwent Class: T01

International Patent Class (Main): G06F-009/38; G06F-012/08

International Patent Class (Additional): G06F-012/08

File Segment: EPI

25/5/10 (Item 6 from file: 350)

DIALOG(R)File 350:Derwent WPIX

011473085 **Image available**

WPI Acc No: 1997-450992/199742

XRPX Acc No: N97-375724

Cache memory system providing set- prediction information for second-level cache - in which second-level set- prediction information is used to select set in N-way off-chip set-associative cache in event of first-level cache miss

Patent Assignee: SUN MICROSYSTEMS INC (SUNM)

Inventor: YUNG R

Number of Countries: 006 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 795828	A2	19970917	EP 97301126	A	19970221	199742	B
EP 795828	A3	19971229	EP 97301126	A	19970221	199818	
JP 10074166	A	19980317	JP 9776701	A	19970313	199821	
KR 97066887	A	19971013	KR 977872	A	19970310	199842	
US 5918245	A	19990629	US 96615662	A	19960313	199932	
EP 795828	B1	20030502	EP 97301126	A	19970221	200330	
DE 69721368	E	20030605	DE 621368	A	19970221	200345	
			EP 97301126	A	19970221		

Priority Applications (No Type Date): US 96615662 A 19960313

Cited Patents: No-SR.Pub; 1.Jnl.Ref; US 5392414; WO 9606390

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 795828	A2	E	14	G06F-012/08	
Designated States (Regional): DE FR GB					
EP 795828	A3			G06F-012/08	
JP 10074166	A		12	G06F-012/08	
KR 97066887	A			G06F-012/08	
US 5918245	A			G06F-012/08	
EP 795828	B1	E		G06F-012/08	
Designated States (Regional): DE FR GB					
DE 69721368	E			G06F-012/08	Based on patent EP 795828

Abstract (Basic): EP 795828 A

The **cache** structure provides set- **prediction** information for a **separate** , second- **level** **cache** . In the event of a first-level cache miss, the second-level set- **prediction** information is used to select the set in an N-way off-chip set-associative cache. An on-chip first-level cache stores set- **prediction** information for the first level cache along with set- **prediction** information for the second level cache.

On each access, the two set **predictors** are stored in different latches, with the first latch being used for current first-level cache access, and the second-level set **predictor** is stored in the second latch for use only in the event of a first-level cache miss.

USE/ADVANTAGE - Providing set- **prediction** information for **predictive** accessing of cache memory. Allows set-associative structure to be used in second-level cache without requiring large number of pins. Enhances performance of multi-threading programs.

Dwg.8/10

Title Terms: CACHE; MEMORY; SYSTEM; SET; **PREDICT** ; INFORMATION; SECOND; LEVEL; CACHE; SECOND; LEVEL; SET; **PREDICT** ; INFORMATION; SELECT; SET; N; WAY; CHIP; SET; ASSOCIATE; CACHE; EVENT; FIRST; LEVEL; CACHE; MISS

Derwent Class: T01

International Patent Class (Main): G06F-012/08

International Patent Class (Additional): G06F-013/00

File Segment: EPI

25/5/11 **(Item 7 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

004567090

WPI Acc No: 1986-070434/198611

XRPX Acc No: N86-051421

Working set pre-etch for level two caches **- is for computing system with three level memory hierarchy and has tags for future use of line based on prior use**

Patent Assignee: IBM CORP (IBMC)

Inventor: ROSENFELD P L; SO K

Number of Countries: 004 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 173893	A	19860312	EP 85110141	A	19850813	198611	B
CA 1228171	A	19871013				198745	
EP 173893	B	19910731				199131	
DE 3583639	G	19910905				199137	

Priority Applications (No Type Date): US 84643931 A 19840824

Cited Patents: 5.Jnl.Ref; A3...8833; No-SR.Pub

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 173893	A	E	23		
	Designated States (Regional): DE FR GB				
EP 173893	B				
	Designated States (Regional): DE FR GB				

Abstract (Basic): EP 173893 B

The system includes a three level memory hierarchy comprised of a first level cache, a second level memory and a main memory. A working set **history** table is included which keeps a record of which lines in an L2 Block where utilised when resident in the L2 cache by use of tags.

When the L2 block, or the material part of the block, is returned to main memory and is subsequently requested, only the lines which were utilised in the last residency are transferred to the L2 cache.

USE/ADVANTAGE - High performance processors. Improved memory access times. (23pp Dwg.No.1/10

Title Terms: WORK; SET; PRE; ETCH; LEVEL; TWO; COMPUTATION; SYSTEM; THREE; LEVEL; MEMORY; HIERARCHY; TAG; FUTURE; LINE; BASED; PRIOR

Derwent Class: T01

International Patent Class (Additional): G06F-012/08

File Segment: EPI